Abstract

A latch architecture for driving unit current cell of a current-steering digital-to-analog converter (DAC) which reduces the drain-source voltage variation of the output current-source transistors and reduces the coupling of unwanted injection of input digital signals as well as clock signals is presented herein. Moreover, this latch helps to achieve lower glitch during code transition with improved dynamic performance. The latch effectively uses the intrinsic RC delay of most transistors within the latch architecture in order to achieve optimal crossing points of complementary control signals. Unwanted input injection or cross-talk is reduced by introducing transistors (904, 906, 932 and 934) that are off during code transitions without compromising the DAC update speed. Conflicts between currently held and new inputs are avoided in an effort to reduce the harmonic distortion. Furthermore, the distortion as a result of the clock signal fed through each transistor in the first and second subcircuit portions cancel each other.